This product is not available for resale

6550

RANDOM ACCESS MEMORY

(1024 X 4)

The 6550 is a high performance, low power, 4K bit, static, read/write random access memory organized as 1024 words by 4 bits per word. It operates on a single 5V power supply and requires minimum buffering and CS decoding.

All interface signal levels are identical to TTL specification, providing high noise immunity and simplified system design. All inputs are purely capacitive MOS loads with no DC current requirements. The output will drive two standard TTL loads and 100 pf.

The 6550 cycle operation is controlled by the $\emptyset_2$ Clock. Addresses are presented to the address pin when $\emptyset_2$ Clock is low and are latched on chip to the rising edge of the $\emptyset_2$ Clock. The Chip Select and Read/Write signals are static and can be presented to the memory at any time. Data In and Data Out signals share common I/O pins and are unable to receive or transmit data when $\emptyset_2$ Clock is high.

The 6550 outputs are in the high impedance state whenever the memory is de-selected, $\emptyset_2$ Clock is low or Read/Write is low.

FEATURES

- 1K × 4 Organization
- Single 5V Power Supply
- Full TTL Compatibility
- Four CS Inputs
- Fully Static Data Storage - No Refreshing
- High Speed - Access Times Down to 200 ns
- Low Operating Power - 450 mW Typical
- Single Phase TTL Level Clock
- High Output Drive - Two Standard TTL Load and 100 pf

PIN CONNECTIONS

Pin	Function	Pin	Function	Pin	Function
1	A_0	8	A_6	15	DB_2
2	A_1	9	A_7	16	DB_3
3	A_2	10	A_8	17	V_{DD}
4	A_3	11	A_9	18	$\overline{CS_4}$
5	A_4	12	R/W	19	$\overline{CS_3}$
6	A_5	13	DB_0	20	CS_2
7	$\emptyset_2$	14	DB_1	21	CS_1
				22	V_{SS}